NXP Semiconductors
Engineering Bulletin

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i.MX 6Solo/6DualLite Application Processor Silicon Revision 1.1 to 1.2/1.3 Comparison

Contents

1. Introduction

This document provides information on changes in the i.MX 6Solo/6DualLite Application Processor between silicon revisions 1.1, 1.2, and 1.3.

2. Changes between revisions 1.1 and 1.2/1.3

Table 1 lists the changes between i.MX 6Solo/6DualLite silicon revisions 1.1 and i.MX 6Solo/6DualLite silicon revisions 1.2 and 1.3. Where an erratum was fixed, the relevant erratum number has been provided along with a high-level description.

Table 1. Changes between silicon revisions 1.1 and 1.2/1.3

Issue number	Description	Impact of change	Silicon Revision Fix	Documented in Silicon Errata Document
—	Silicon revision 1.1: Last letter of the part number is “B”. Silicon revision 1.2: Last letter of the part number is “C” and the maskset ID is “2N81E”. Silicon revision 1.3: Last letter of the part number is “C” and the maskset ID is “3N81E”. See the device datasheet nomenclature diagram for more details on how to read the part number.	n/a	n/a	Rev. 5
—	Updated contents of Chip Silicon Version register (USB_ANALOG_DIGPROG): 0x00610001 for silicon revision 1.1 0x00610002 for silicon revision 1.2 0x00610003 for silicon revision 1.3	U-boot reads the ROM revision contents to determine the silicon revision. The ROM revision number may not match the silicon revision number.	Updated in 1.2 and 1.3	n/a
—	ROM version number at address 0x48: “0x11” for silicon revision 1.1 “0x12” for silicon revision 1.2 “0x13” for silicon revision 1.3	Only affects software that reads the ROM version	Updated in 1.2 and 1.3	n/a
ERR007117	ROM: When booting from NAND flash, enfc_clk_root clock is not gated off when doing the clock source switch.	The workarounds documented in the errata are not required for revision 1.2.	Fixed in 1.2	Rev. 3
ERR007122	ROM: TZASC_ENABLE fuse bit is coded in ROM as bit 24 at location 0x460 whereas the fuse map defines it as bit 28.	The workarounds documented in the errata are not required for revision 1.2.	Fixed in 1.2	Rev. 3
ERR007220	ROM: NAND boot may fail due to incorrect Hamming checking implementation in the ROM code.	The workarounds documented in the errata is not required for revision 1.2.	Fixed in 1.2	Rev. 3
ERR005768	ROM: In rare cases, secondary image boot flow may not work due to incorrect sampling of the	None (improvement)	Fixed in 1.3	Rev. 5

Table 1. Changes between silicon revisions 1.1 and 1.2/1.3

Issue number	Description	Impact of change	Silicon Revision Fix	Documented in Silicon Errata Document
	WDOG reset.			
ERR007926	ROM: 32 kHz internal oscillator timing inaccuracy may affect SD/MMC, NAND, and OneNAND boot	None (improvement) - No hardware or software change required.	Fixed in 1.3	Rev. 4
ERR008506	ROM: Incorrect NAND Bad Block management	None (improvement)	Fixed in 1.3	Rev. 5
ERR008057	MMDC: Skew difference of up to 150 ps observed on SDCLK0, DQS0 and DQS7 differential traces	None (improvement) - No hardware or software change required.	Fixed in 1.3	Rev. 4

3. Software changes from revision 1.1 to 1.2

The i.MX 6Solo/6DualLite ROM code has been updated between revisions 1.1 and 1.2. The ROM code update addressed the silicon errata listed in Table 1. Read below for details on software patches that may need to be applied to your system software when moving from revision 1.1 designs to revision 1.2 designs.

3.1. Chip revision support

To ensure that the new chip revision can be read back from the chip, the following patch should be applied.

- ENGR00286181 ARM®: i.MX6: add more chip revision support.

http://git.freescale.com/git/cgit.cgi/imx/linux-2.6-imx.git/commit/?h=imx_3.0.35_4.1.0&id=21464af587382ec1841d5fd346eaf359827c6142

3.2. U-boot plug-in mode or secure boot

The ROM code of i.MX 6Solo/6DualLite revision 1.2 changed the ROM_API_TABLE_BASE_ADDR and HAB_API table address (4 byte offset increase).

If using u-boot plug-in mode or secure boot, the following two patches must be applied to your u-boot.

1. ENGR00285890 imx6:plugin: update the ROM_API_TABLE_BASE_ADDR for plug-in code.

http://git.freescale.com/git/cgit.cgi/imx/uboot-imx.git/commit/?h=imx_v2009.08_3.0.35_4.1.0&id=a929825706b5e1508 b29d8ae2a2afb2fcbb2de19

NOTE

The plug-in mode patch is board dependent, which means you must apply similar fixes onto your plug-in mode code by referring to the details in the above patch.

2. ENGR00287268 mx6: fix the secure boot issue on the new tapout chip

http://git.freescale.com/git/cgit.cgi/imx/uboot-imx.git/commit/?h=imx_v2009.08_3.0.35_4.1.0&id=424cb1a79e9f5ae4e de9350dfb5e10dc9680e90b

NOTE

The secure boot patch is SoC dependent, so the patch can be applied directly.

The NXP external uboot-imx.git has the patches to correct the ROM_API_TABLE_BASE_ADDR and HAB_API table address. The patches have been tested with the NXP development systems and BSP.

The two patches have been pushed to imx_v2009.08_3.0.35_4.1.0 branches of NXP external uboot-imx.git.

4. Software changes from revision 1.2 to 1.3

No software changes required to migrate from revision 1.2 to 1.3.

5. Revision history

Table 2. Revision history

Revision number	Date	Substantive changes
0	12/2014	Initial release
1	5/2015	Addition of silicon revision 1.3 information.
2	6/2015	Update to the second row of Table 1
3	10/2015	Additional update to the second row of Table 1
4	11/2015	Update to Table 1
5	7/2017	Update to the second row of Table 1 Third line removed in Table 1.

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